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From: Bradley J. Berezna (Reg. No. 33,474)

Date: July 18, 2005 Time: 1:49 p.m. PDT

Operator: Brad Berezna Matter: 07716.P001

Number of pages including cover sheet: 3

In re Patent Application of: Kenneth Tseng Attorney Docket No.: 07716.P001

Application No.: 10/078,732 Filed: February 19, 2002

For: Variable Stage Ratio Buffer Insertion for Noise Optimization in a Logic Circuit

Enclosed are the following documents: Response to Election Requirement.

Please call Bradley J. Berezna, should you have any questions regarding the above.

Respectfully Submitted,

Bradley J. Berezna

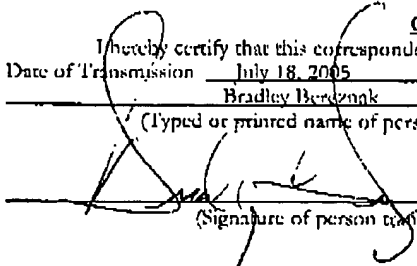
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Attorney Docket No. 07716.P001

JUL 18 2005**PATENT****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

TSENG, KENNETH

Serial No.: 10/078,732

Filing Date: February 19, 2002

For: **VARIABLE STAGE RATIO BUFFER
INSERTION FOR NOISE OPTIMIZATION
IN A LOGIC CIRCUIT**

Examiner: Tat, Binh C.

Art Unit: 2825

Response to Election RequirementCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the restriction requirement mailed June 30, 2005 having a period for response of one month, Applicant responds as follows: